Assessment of Selected CERES Electronic Component Survivability under Simulated Overvoltage Conditions

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Introduction

In August, 1998 a Clouds and the Earth's Radiant Energy System (CERES) instrument telemetry housekeeping parameter generated a yellow warning message that indicated an on-board +15V Data Acquisition Assembly (DAA) power converter deregulation anomaly. An exhaustive investigation was undertaken to understand this anomaly and the long-term consequences which have severely reduced CERES operations on the Tropical Rainfall Measuring Mission (TRMM) spacecraft. Among investigations performed were ground tests that approximated the on-board electronic circuitry using a small quantity of flight identical components exposed to maximum spacecraft bus over-voltage conditions. These components include monolithic integrated microcircuits that perform analog signal conditioning on instrument sensor signals and an analog-to-digital converter (ADC) for the entire DAA. All microcircuit packages have either a bipolar silicon design with internal current limiting protections or have a complementary metal oxide semiconductor (CMOS) design with bias protections. Ground tests that have been running for approximately 8 months have indicated that these components are capable of withstanding as much as twice their input supply voltage ratings without noticeable performance degradation. These data provide CERES operators with confidence of being able to continue science operations over the remaining life of the TRMM mission. This paper will discuss this anomaly and some possible causes, a simulator of affected electronics, test results, prognosis for future CERES operations, and conclusions.

Power Converter Anomaly and Possible Degradation Mechanisms

The power converter that drives the CERES data acquisition electronics takes the fused spacecraft +28V supply bus voltage and converts it into a near constant regulated +15V output. Due to a non-disclosure agreement with the converter manufacturer, exact details of the converter design and specific anomaly causes cannot be revealed or discussed. However, based on experience with commercial converters, some generalizations can be made. Normally, output voltage level regulation is accomplished via an internal feedback loop, which when degraded, allows the output voltage to increase above the nominal specifications. On CERES, an anomaly has occurred that makes the output sensitive to both temperature (to normal orbital thermal cycles) and input voltage transients. This can be seen in Figure 1. The top trace is the TRMM spacecraft (S/C) bus voltage during three consecutive 92 minute orbits, (use right-side scale for S/C voltage). The lower trace is the output of the affected power converter, (refer to the left-side scale for converter output voltage levels). Furthermore, the downstream DAA signal conditioning and ADC components are considered to be potentially sensitive to excessive supply voltage (Vcc) levels. The slightest effects could corrupt the entire instrument science and housekeeping data output.
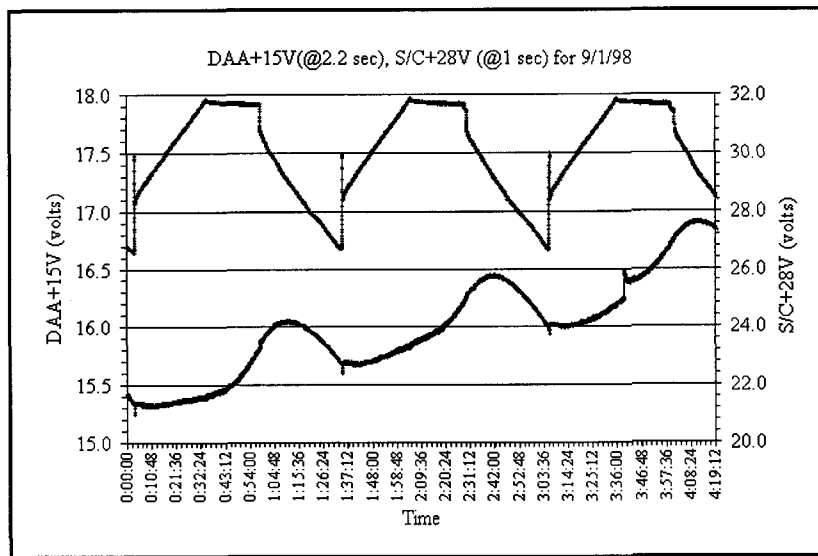
Figure 1. Spacecraft Input and Converter Output Voltages

To understand this anomaly and to correlate its behavior to the telemetry data, several spare converters from similar manufacturing lots and dates underwent environmental tests that simulated possible orbital conditions that might have caused a regulation degradation. For example, some converters were tested for sensitivity to proton induced radiation damage. However, in-orbit exposure levels were found to be two orders of magnitude below the damage threshold level. Additionally, some exposed converters were subjected to simulated spacecraft bus voltage levels using a variable (0-40 V) DC, 20 amp power supply with an equivalent CERES power load. A series pass transistor pair circuit was used to modulate the power to a power converter under test with a replica of the TRMM spacecraft orbital bus power envelope. This replica was achieved by programming a Wavetek 75A programmable waveform generator that approximated the positive slope, steady state, and negative slope portions of the bus waveshape and was applied to the base of the series pass transistor pair. Using a duty cycle of 9.2 seconds (instead of a 92 minute orbital period) during testing, the subjected power converter failed audibly while bias adjustments were being made. Post test de-lidding examination showed the tiny ball bond wire lead from the input switching power metal oxide semiconductor field effect transistor (MOS-FET) to be intact but discoloration was observed on the MOS-FET switching transistor under the bonding wire pad. Presumably the internal switching transistor had failed due to overheating from repeated start-up power dissipation.

The threat to CERES electronic components can be further understood with a review of silicon integrated circuit (IC) die failure modes. These failures are typically classified as electrical, mechanical or physical-chemically (e.g.,corrosion, electro-migration) induced modes. Electrical device overvoltage failures may occur with overheating. This can be due to a possible dielectric (or oxide) breakdown, or due to excessive current density in the semiconductor junctions or the ball bond wires. For a silicon IC, silicon dioxide is the predominate dielectric and its dielectric strength exceeds several million volts per centimeter. For dielectric breakdown, the critical voltage level is proportional to the cube of the electric field strength, expressed in units of megavolts per centimeter near the breakdown portion of the voltage-current (V-I) curve (1).

Further, the oxide thickness greatly influences the breakdown potential, with pinhole defects or thin layers representing premature failure zones (characteristics typically associated with memory or FET gates). Considering that dielectric breakdown phenomena typically occur in milliseconds, component testing with overvoltage conditions over minute or hourly test intervals are eternities, relative to the rate of the dielectric breakdown (1) mechanism. And due to thick oxide layers in the devices tested, a doubling of the input supply voltage (Vcc) won't remotely approach the dielectric breakdown level. Excessive current densities from high supply volt levels could also be expected to induce thermal failure from excessive component heating. In extreme cases, thermal failure modes can be caused by metallization melting, dopant migration, or simply exceeding the glass transition temperature (melting point) of the die attachment or bonding wire adhesives.

Mechanically induced failures are typically separations between the die and interconnection wires and the package lead frames. For hybrid components, separations can occur due to weak bonding adhesives between subcomponents and the die substrate. For ICs, the interconnection wire integrity between the die and the package lead frame is an important factor. The specification typically used is the mean time to failure (MTF), shown below, as given by M. Pecht, et al, (2).

$$MTF = (A*exp^{(1.2/KT)}) / (8.5*E^{-10}*(J)^2)$$

where:
  A = Wire interconnect cross sectional area
  T = Temperature
  K = Boltzman constant
  J = Current density

Physical-chemically induced failures typically involve the intermetallic interfaces (e.g., bond wire contacts with die metallization). The rate at which intermetallic failures proceed is influenced by temperature and is dependent upon the activation energy levels of the specific materials. Since activation energies determine the slope of the mean-time-to-failure (MTF), physical-chemical failures are generally not a concern below ambient temperatures of 150° C. This is due to the dominate lower activation energies effects rather than temperature effects.

CERES Benchtop Circuit Simulator

In addition to investigating and understanding the power converter anomaly, an investigation was needed to assess the operational robustness of the down-stream electronics to unregulated converter output effects. Of particular interest was how well these electronics could withstand Vcc levels approaching the spacecraft input bus voltage levels, which theory suggests the electronics should accommodate. Computer based modeling of electronic circuits is usually restricted to the nominal values indicated by the component manufacturers. To numerically predict the performance of a component as it is subjected to overvoltage conditions is difficult without the detailed device schematics. Since this proprietary information is not readily available, a more expedient and reliable alternative was to assemble a mock-up of the DAA affected circuit (see Figure 2) using flight equivalent components.

Three redundant, commercially available personal computer (PC) analog to digital (ADC) adapter
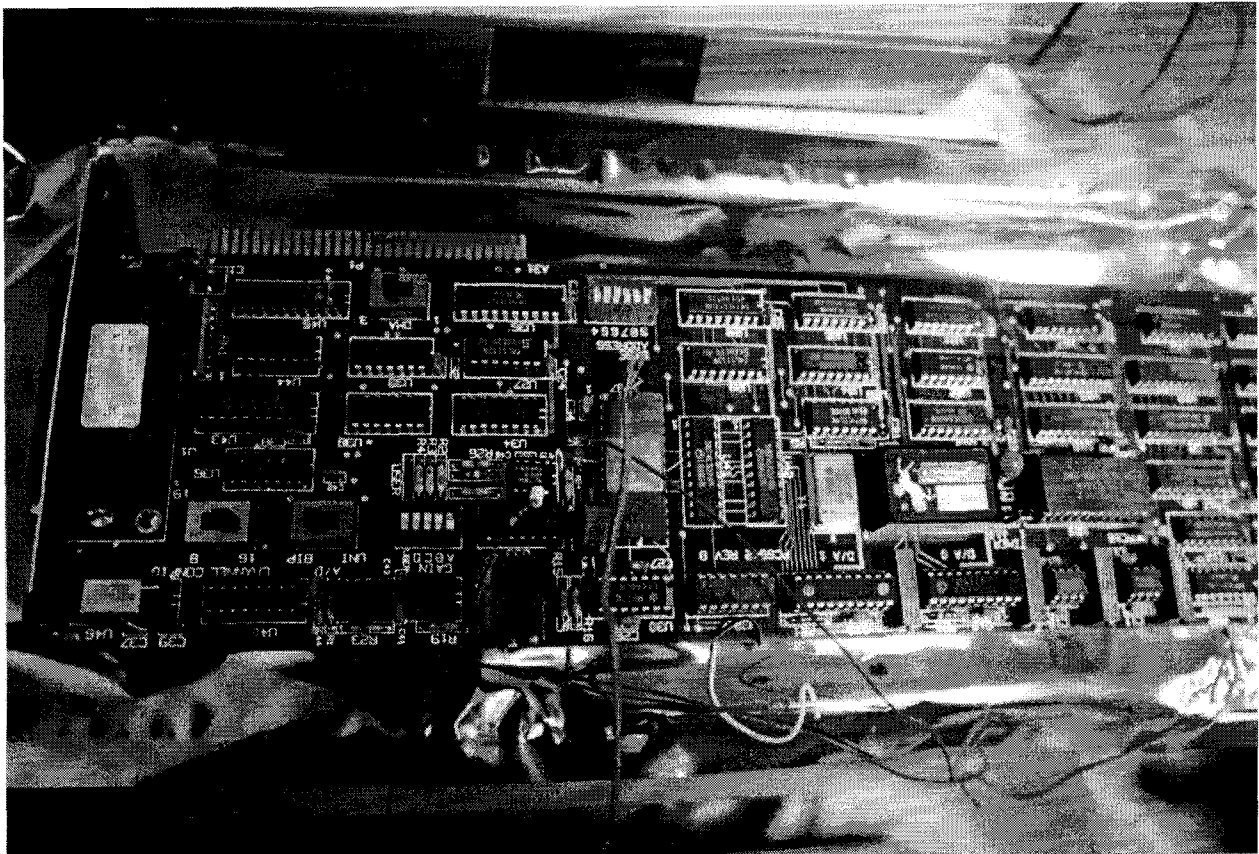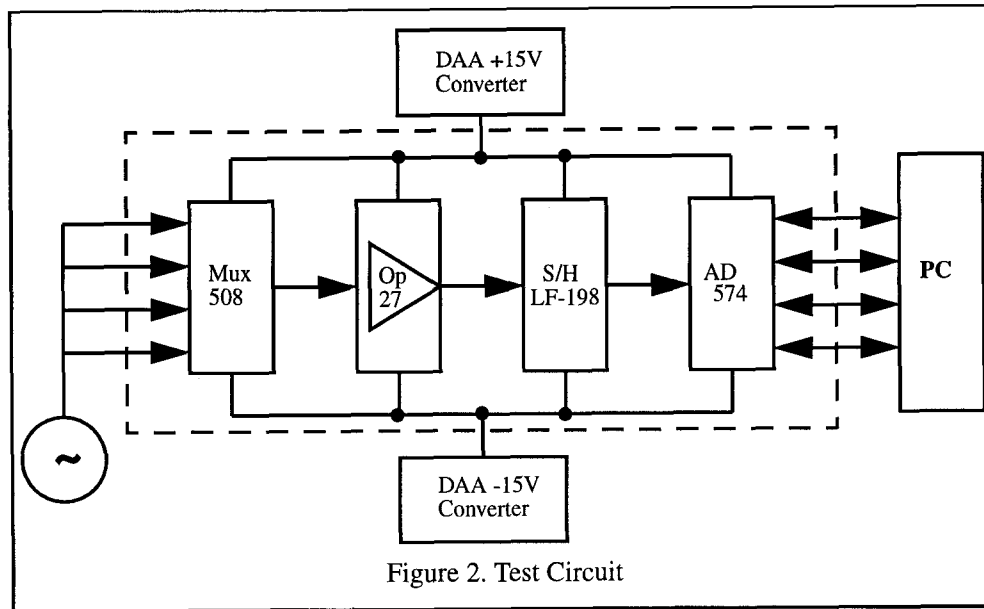
Figure 2. Test Circuit

Figure 3. DAS-16 Card

cards with scanning software were used to provide a test suite for dynamic data collection. A prototyping card was also used to study components not easily adaptable to the PC card sockets. The DAA signal conditioning components include monolithic ICs (e.g., switchers and amplifiers) that condition small instrument sensor signals and an analog-to-digital converter (ADC). For CERES, the ADC encodes all the radiometric science and housekeeping parameter signals for input to a Data Acquisition Processor (DAP). All packages have either a bipolar silicon design

with internal current limiting protections or a CMOS design with bias protections.

A calibration input signal was provided by a HP 6114A power supply. This unit allows for calibration levels to be manually selected by thumbwheel switches in 1 mV increments. The CERES sample & hold (S/H), multiplexer (Mux), operational amplifiers (OP-Amps) and ADC were approximated by using a modified Keithley/Metrabyte DAS-16 card in lieu of the DAP (see Figure 3). Output levels were observed and recorded for calibrated input levels alternating between 0 volts and 2.5 volts. External power supplies, with current monitoring capabilities, were substituted for the power converter components. During testing, the signal condition components were operated within manufacturer's published supply voltage specifications, albeit at or slightly over the upper limit. Since the IC biasing networks are designed to provide for stable operation over a very wide temperature and supply voltage range, the applied input component power was -15 volts and +29 volts, except during periodic calibration tests where the +Vcc supply was varied between 11 to 29.5 volts.

Test Results

The performance of both individual components and the complete circuit was evaluated using two techniques. Individual components were evaluated by measuring their voltage-current (V-I) performance using a varying Vcc supply. The overall circuit was evaluated using input calibrated signal to output digital count transfer ratios for both a varying Vcc supply range and under worst-case, steady-state overvoltage conditions. The Vcc power supply ranged from +11V to +29.5 volts. In addition, actual device and operating temperature dissipation measurements were also noted and compared to specifications during maximum DAA power supply voltage conditions.

For the individual microcircuit components, their V-I curves are shown in Figures 4-6. These curves show that for a varying Vcc supply, ranging from +11V up to the worst-case +29.5V overvoltage level, the current draw followed the manufacturer's expected performance specifications. The thermal case dissipations were noted, under worst-case Vcc, and the results are summarized in Table 1 below. An illustration of the component case dissipation as a percent of the total dissipation is shown in Figure 7.

Table 1: Device Dissipations

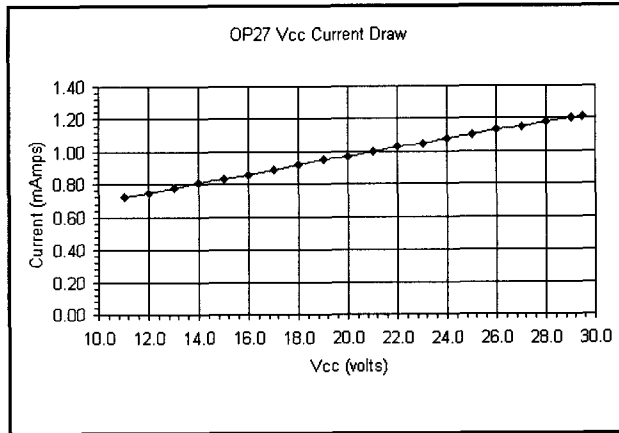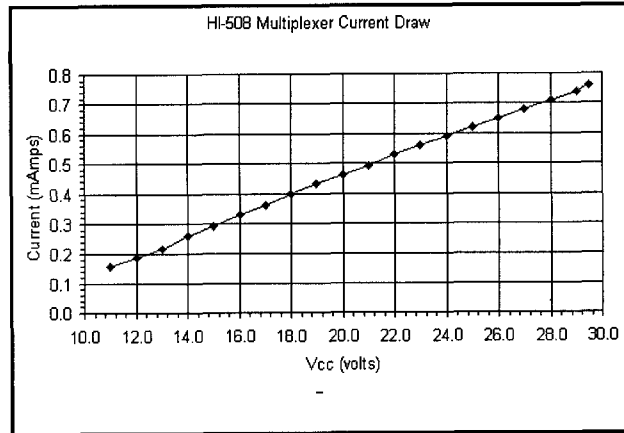| Component	Component	Rated	Applied	Nominal	Mil. Spec. Temperature		Dissipation	maximum	% of
Device	Function	Vcc (V)	Vcc (V)	Icc (mA)	Range (°C)		(mWatt)	(mWatt)	Maximum
PMI OP27	Amp	18	29.5	3.3 - 5.6	-55	125	48.15	140	34%
AD574	ADC	16.5	29.5	1.4	-55	125	309	1000	37%
LF198	Mux	18	29.5	4.5 - 6.5	-55	125	25.5	500	5%
Hi508/883	S/H	22	29.5	2.4	-55	125	26.75	1009	2.7%

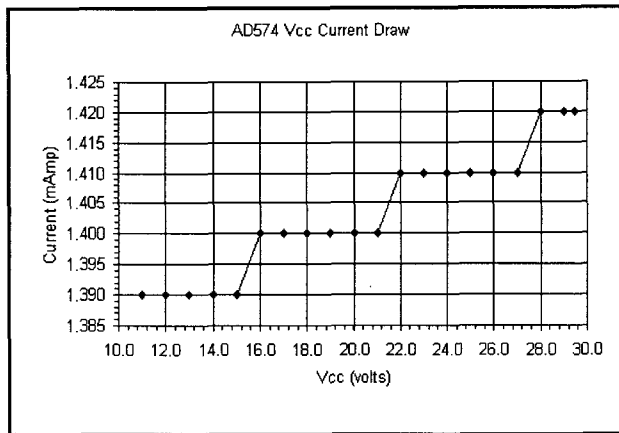Figure 4. OP27 V-I Curve

Figure 5. Hi508 V-I Curve
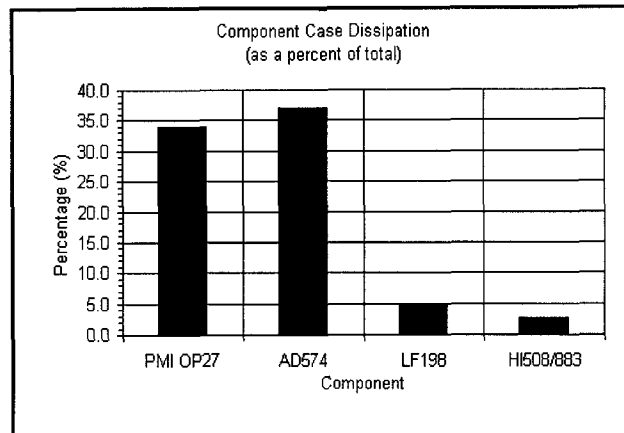

Figure 6. AD574 V-I Curve

Figure 7. Thermal Dissipation Percent of Total

These data support the observations that the amplifier and sample/hold circuits were found to employ internal current limiting coupled via thermal feedback elements. For example, at positive supply levels above the predicted maximum overvoltage, the V-I curves were found to exhibit hysteresis due to current-limiting as the device temperature increases slightly from self heating. However, the monolithic AD574 is somewhat different as it employs an integrated zener diode voltage reference source with an intrinsic current limiting circuit. This limits the input current to about 1.4 mAmp over the Vcc supply voltage range. The internal ADC reference voltage level provided by the zener stabilized circuitry remained at +9.66 volts over the same range. (For CERES, the +10 volt reference voltage is supplied by a separate precision reference voltage source.) In addition, this current limiting circuit helps to limit thermal dissipation, improve thermal stability, and provide immunity of the precision reference voltage to input Vcc voltage variations. The only measurable overvoltage related thermal effect on the ADC was to raise the temperature about 0.1 $^{\circ}$C per volt above the nominal quiescent equilibrium temperature as the supply is increased above the nominal+15 volt. Therefore, the results from these case dissipation evaluations can be useful for characterizing the components at risk.

To evaluate the overall circuit, a calibrated input signal was applied to obtain output digital count transfer ratios for both a varying +Vcc supply range and under worst-case, steady-state +29.5

overvoltage conditions. Using a 0.0V input, the ADC digital output level was 2048 counts and for a 2.5V input, the digital output was 3073 counts. From this, a voltage-to-count transfer ratio can be computed to be 410 counts (3073-2048) over 2.5 volts. This yields a sensitivity ratio of 2.44 millivolts per count for the overall ADC encoder circuitry. Then with these same input signals, the circuit +Vcc was again varied between +11V and 29.5V. The resulting voltage-to-count ratio is shown in Figure 8. Lastly, by applying a maximum predicted overvoltage Vcc of +29.5V during an 8 month period, the entire signal conditioning and ADC circuit was found to tolerate this condition without the end-to-end voltage-to-count transfer ratio deviating by more than 1 LSB. This is within the manufacturer's performance specifications.
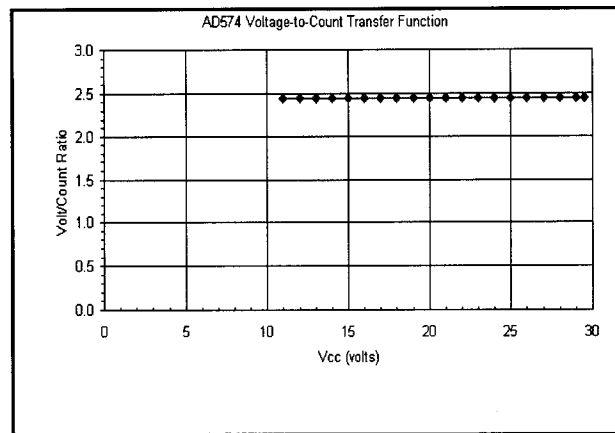

Figure 8. Circuit Transfer Ratio

The signal conditioning and ADC fidelity test results shown indicate that the components could survive full unregulated spacecraft supply voltage levels without adverse effects upon system accuracy or component life expectancy. The fact that the conversion level remained constant regardless of the Vcc input level, gives confidence that the CERES on-board affected circuitry offset and sensitivity stability will maintain calibration and that the science data will not be corrupted.

Conclusions

The CERES DAA +15 volt power converter is expected to continue degrading during future operational periods. This degradation is anticipated to cause the nominal +15 volt Vcc source to climb to the near spacecraft bus voltage levels of approximately +29.5 volts. To evaluate the long-term effects on the down-stream electronics, a benchtop circuit simulation scenario was developed using comparable flight qualified analog electronics. Simulations were performed using on-going tests of worst case expected overvoltage level and periodic on-off cycling.

The benchtop components showed a remarkable robustness to overvoltage conditions. The benchtop overvoltage tests have been on-going for 8 months and continues as of this writing. The components have exhibited no excessive current or heat dissipations beyond the manufacturer's published maximum values. The V-I tests results revealed linear relationships and case temperatures that remained at ambient or 1° C above for the ADC converter values. No shifts in the voltage-to-counts transfer ratio were observed for the analog-to-digital signal conversion

circuit. This benchtop performance has been verified against the on-orbit instrument telemetry data. Specifically, the in-orbit radiometric calibration measurements show no effects when the on-board DAA+15V converter output drifted as high as +19.9 volts.

As the in-orbit DAA +15V deregulation anomaly progresses, the ability of the telemetry system to monitor the +15V levels will be limited whenever this regulator exceeds the +20V maximum ADC quantization range. Ground testing of comparable components yields confidence that the critical circuitry will not only survive, but will continue to produce accurate science data from the instrument.

References

1. I. C. Chen and Chenming Hu, "Accelerated Testing of Time-Dependent Breakdown of SiO2", IEEE Electron Device Letters, Vol. EDL-8, No. 4, April 1997.

2. M. Pecht, P. Lall and E. B. Hakim, Quality and Reliability Engineering International CALCE Electronics Packaging Research Center, Univ. of MD, US Army, Labcom, "The Influence of Temperature on Integrated Circuit Failure Mechanisms", Vol. 8, No. 3, pp. 167-175, May-June 1992, John Wiley & Sons Ltd.